FIG. 1

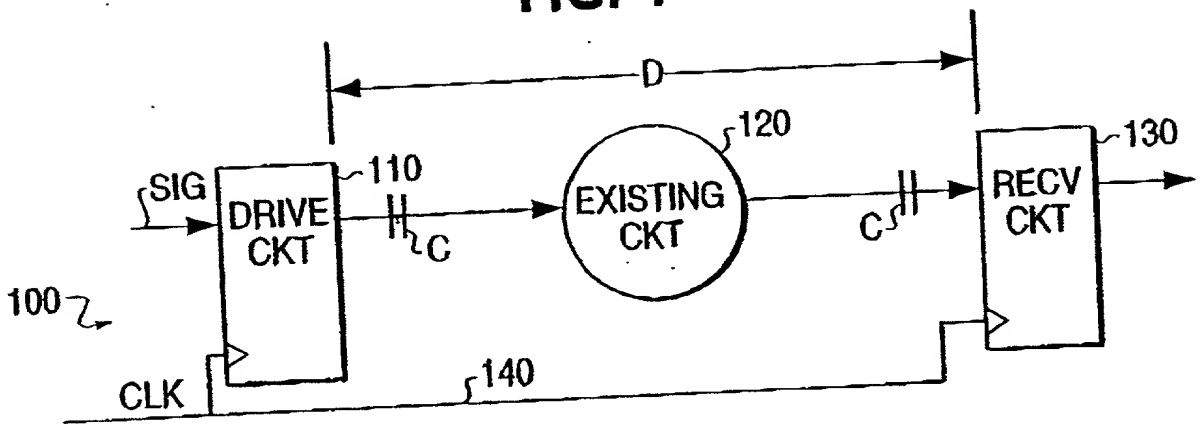
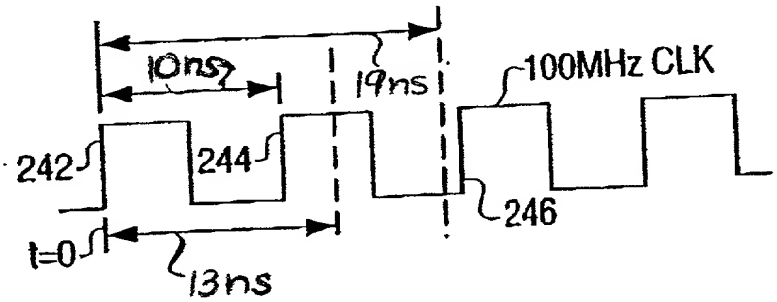

D
120
130
SIG
DRIVE CKT
110
C
EXISTING CKT
C
RECV CKT
100
CLK
140

FIG. 2


10ns
19ns
100MHz CLK
242
244
246
t=0
13ns

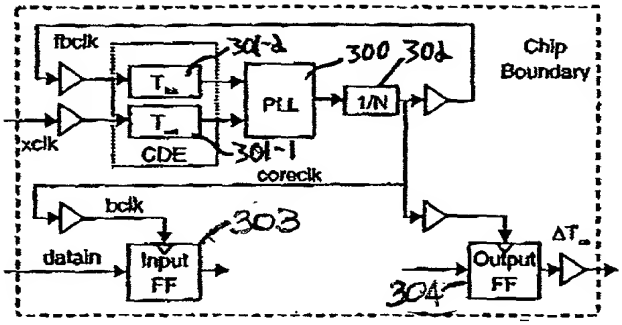


FIG. 3

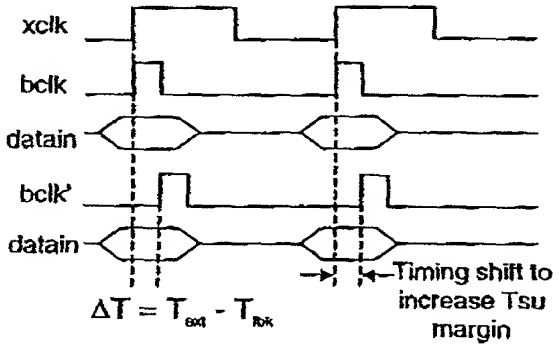


FIG. 4

Fix	Margin On	Action	Add ΔT_{co}
Tsu	Tco,max, Th	$\uparrow T_{ext}$	-
Th	Tco,min, Tsu	$\uparrow T_{fbk}$	-
Th	-	$\uparrow T_{fbk}$	Yes
Tco,max	Tsu	$\uparrow T_{fbk}$	-
Tco,min	Th	$\uparrow T_{ext}$, $\downarrow T_{fbk}$	-
Tco,min	-	$\uparrow T_{ext}$	Yes

FIG. 5

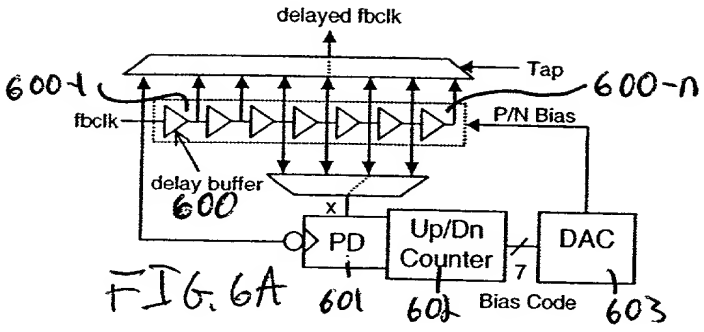


FIG. 6A

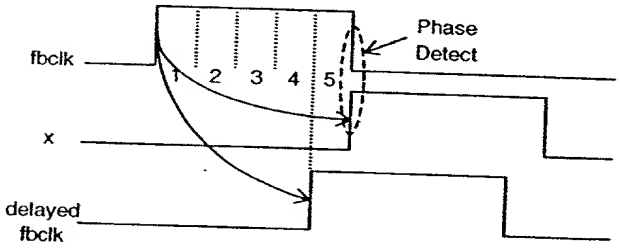


FIG. 6B

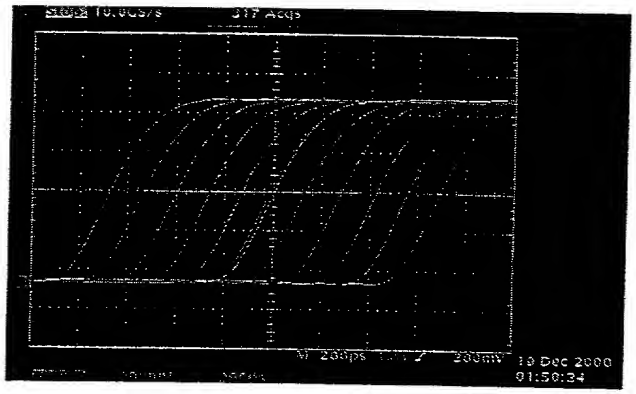
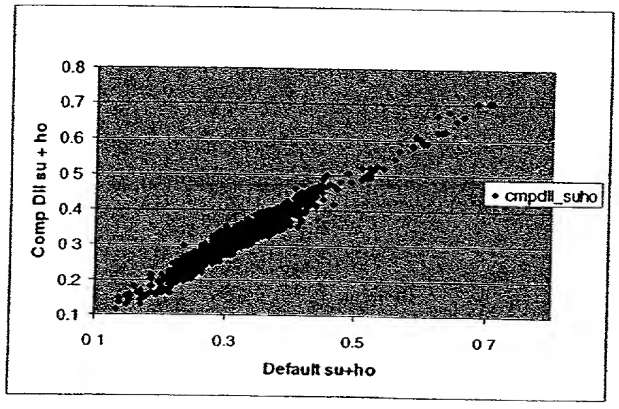


FIG. 7

FIG. 8



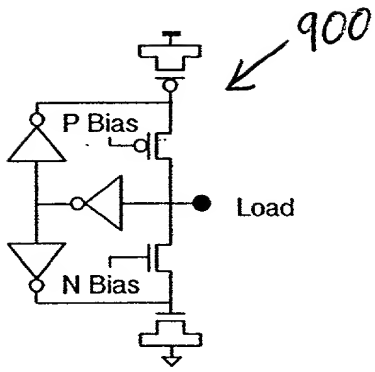


FIG. 9

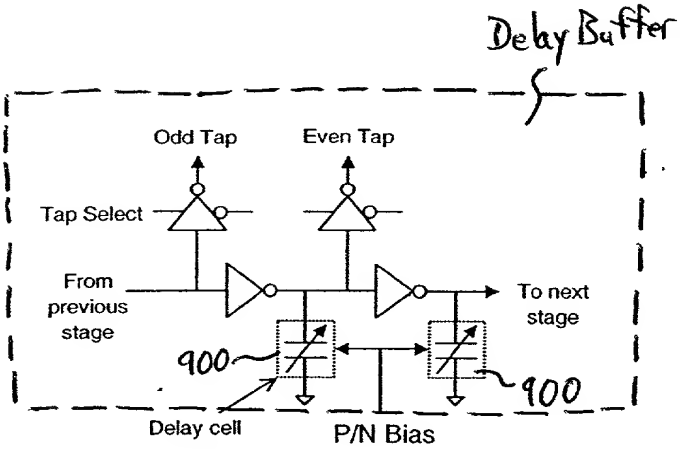


FIG. 10

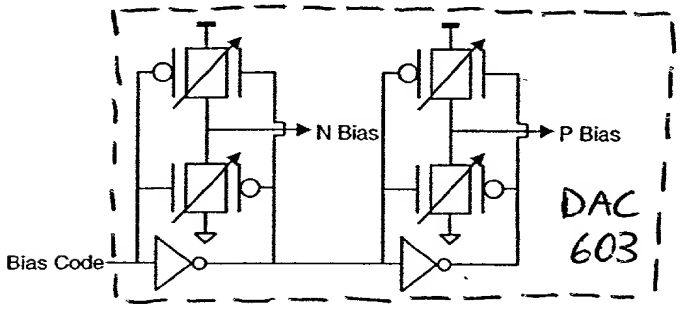
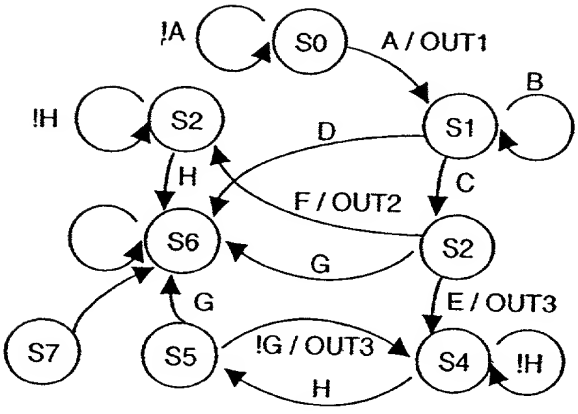


FIG. 11



A	: Pwrgd
B	: (!CDElock·PLLlock) + !PLLlock
C	: CDElock·PLLlock·FSMen
D	: PLLlock·!FSMen
E	: !TapEqFuse·!Mlock
F	: !TapEqFuse·Mlock
G	: TapEqFuse
H	: PLLlock
OUT1	: if (FSMen), Tap = 000; Else Tap = Fuse Value
OUT2	: Tap = Fuse Value
OUT3	: Tap = Tap + 1

FIG. 12

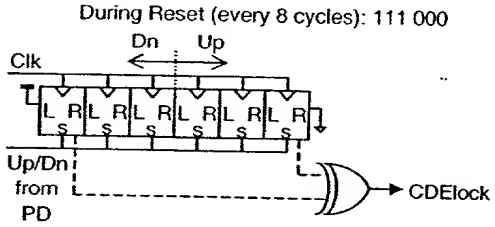


FIG. 13

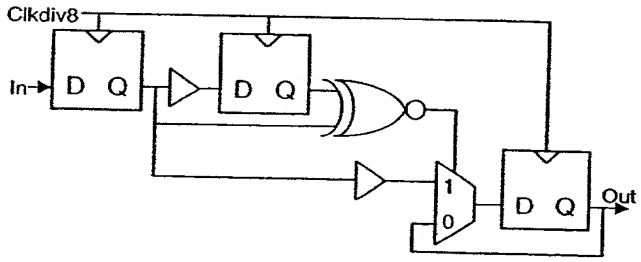


FIG. 14

Condition	Voltage	Bias Code
95nm, 95°C	1.10V	1000101
(Slow)	1.25V	0110011
	1.40V	0101100

Condition	Voltage	Bias Code
75nm, 5°C	1.10V	0101110
(Fast)	1.25V	0100101
	1.40V	0011101

FIG. 15

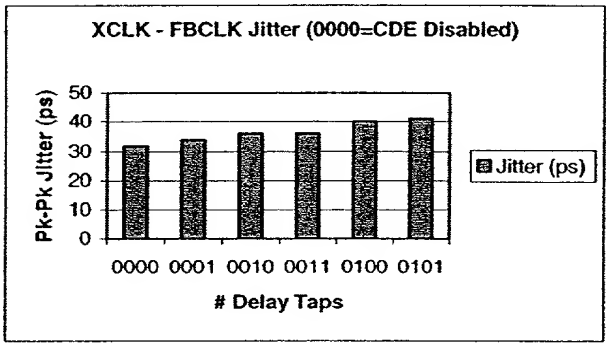


FIG. 16

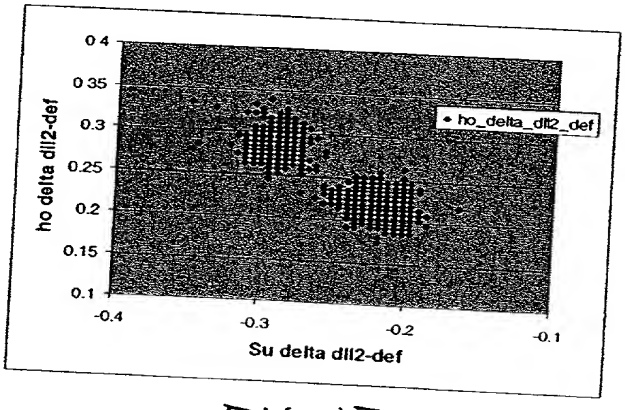


FIG. 17